IN THE CLAIMS:

Rewrite the claims as follows.

1-20. (canceled)

21. (New) A method of operation in a dynamic random access memory device that includes banks of dynamic memory cells, the method comprising:

receiving a self refresh command, wherein the memory device performs a refresh operation in response to the self refresh command;

refreshing rows of the memory cells located in each of the banks during the refresh operation; and

selecting a refresh frequency for the refresh operation such that the refresh frequency is minimized to conserve power consumed by the memory device while being sufficient enough to refresh the rows of the memory cells.

22. (New) The method of claim 21, wherein selecting the refresh frequency includes configuring an oscillator that generates an internal refresh clock.

23. (New) The method of claim 22, wherein the internal refresh clock triggers an internal refresh driver that energizes sense amplifiers corresponding to a row being refreshed during the refresh operation.

24. (New) The method of claim 22, wherein configuring the oscillator includes blowing a fuse.

25. (New) The method of claim 22, wherein the oscillator is configured in response to a device configuration signal.

26. (New) The method of claim 22, wherein the oscillator is configured by dividing the output of the oscillator to generate a divided clock signal that is selected as the internal refresh clock

27. (New) The method of claim 21, further including incrementing a counter that holds a row address corresponding to which of the rows of the memory cells located in each of the banks being refreshed.

28. (New) The method of claim 27, wherein a row corresponding to the row address is simultaneously refreshed in each of the banks before incrementing the counter.

29. (New) The method device of claim 27, wherein a row corresponding to the row address is sequentially refreshed in each of the banks before incrementing the counter.

30. (New) A dynamic random access memory device comprising:

a memory core including a plurality of addressable banks, wherein each addressable bank of the plurality of addressable banks includes dynamic memory cells;

a plurality of sense amplifiers coupled to the memory core, to refresh the dynamic memory cells in each addressable bank in response to a self refresh command; and

a refresh counter to generate row addresses corresponding to rows of the dynamic memory cells in each addressable bank to be refreshed, wherein the frequency in which the row addresses are generated is selectable such that the refresh frequency is minimized to conserve power consumed by the memory device while being sufficient enough to refresh the dynamic memory cells in each addressable bank.

31. (New) The dynamic random memory device of claim 30, wherein the row addresses are applied to each addressable bank.

32. (New) The dynamic random access memory device of claim 31, wherein the row addresses are applied simultaneously to each addressable bank.

33. (New) The dynamic random access memory device of claim 32, wherein the row addresses are applied in sequence to each addressable bank.

34. (New) The dynamic random access memory device of claim 30, further including an oscillator coupled to the refresh counter to generate a clock signal that triggers refreshing of

the rows of the dynamic memory cells in each addressable bank, wherein the frequency in signal.

35. (New) The dynamic random access memory device of claim 34, further including a fuse, coupled to the oscillator, wherein the frequency of the clock signal is changed by blowing the fuse.

36. (New) The dynamic random access memory device of claim 34, further including a divider circuit coupled to the oscillator, wherein the frequency of the clock signal is changed by selecting a divided version of an output of the oscillator.

37. (New) A dynamic random access memory device including a memory core having a plurality of addressable banks, wherein each addressable bank of the plurality of addressable banks includes dynamic memory cells, wherein the memory device comprises

a plurality of sense amplifier means for refreshing the dynamic memory cells in each addressable bank in response to a self refresh command; and

a refresh counter means for generating row addresses corresponding to rows of the dynamic memory cells in each addressable bank to be refreshed, wherein the frequency in which row addresses are generated is selectable such that the refresh frequency is minimized to conserve power consumed by the memory device while being sufficient enough to refresh the rows of the dynamic memory cells.

38. (New) The dynamic random memory device of claim 37, wherein the row addresses are applied to each addressable bank.

39. (New) The dynamic random access memory device of claim 38, wherein the row addresses are applied simultaneously to each addressable bank.

40. (New) The dynamic random access memory device of claim 38, wherein the row addresses are applied in sequence to each addressable bank

41. (New) The dynamic random access memory device of claim 30, further including oscillating means for generating a clock signal that triggers refreshing of the rows of dynamic

memory cells in each addressable bank, wherein the frequency in which the row addresses are generated is selectable by changing the frequency of the clock signal.

42. (New) The dynamic random access memory device of claim 30, further including fuse means for selecting the frequency in which the row addresses are generated.